

ABSTRACT OF THE DISCLOSURE

A decoder circuit of the present invention, mounted on an integrated circuit, decodes input voltage V_{in} supplied to a single external input terminal into three or more control outputs, and an object of the present invention is to reduce the size of a chip. The foregoing decoder circuit includes: a P-type transistor in which an emitter is connected to a power source line of high level, a base is connected to the external input terminal, and a collector is an output terminal of a first control output; and an N-type transistor in which an emitter is connected to a power source line of low level, a base is connected to the external input terminal, and a collector is an output terminal of a second control output, and decodes the control outputs to three or more sets of data by carrying out logic operations. Therefore, as compared to the case of using a comparator requiring many transistors, a constant current source, and other elements, one each transistor is required for each of the two control outputs to be generated. This facilitates size reduction of a chip.